REMARKS

New claim 14 has been added. Claims 1-14 are currently pending. The Examiner's rejections are traversed below.

On page 2 of the Office Action, the Examiner rejected claims 1-5 and 7-13 under 35 U.S.C. § 102(b) as being anticipated by "Cost-Effective Generation of Minimal Test Sets for Stuck-at Faults in Combinational Logic Circuits," IEEE, Dec. 1995, pp.1496-1504 (Kajihara).

Kajihara is directed to test generation procedures for combinational circuits to achieve fault coverage. According to Kajihara, the procedures are aimed at generating small test sets, which are important for reducing test storage requirements and test application time, according to Kajihara. Kajihara further describes a dynamic test compaction technique called "double detection." Kajihara uses double detection to collect information that will allow redundant tests to be dropped by fault simulating the tests generated. Kajihara also uses essential faults of tests in a test set to be compacted as the target faults in the generation of the additional test vectors that will replace the test vectors in the given test set.

In at least one embodiment of the present invention, a selection device selects essential test stimuli from among subsets of the set of test stimuli after mapping between the test stimuli and the faults has been established by the simulation. An elimination device eliminates redundant test stimuli from among subsets of test stimuli after selection of essential test stimuli from each subset. *See* claim 1, for example.

Applicants respectfully submit that independent claims 1, 10, 11, 12, and 13 are patentable over Kajihara, as Kajihara fails to disclose, "an elimination device *eliminating redundant test stimuli* from among subsets of test stimuli *after selection of essential test stimuli* from each subset," as recited in claim 1, for example.

In contrast to the present invention, Kajihara clearly states that the essential faults can be extracted by using the fault list that results from the double detection procedure, that is, the procedure which allows redundant tests to be dropped by fault simulating. As the essential faults use the fault list resulting from the double detection procedure, the double detection procedure, that is, the procedure relating to redundant tests, occurs before the essential faults procedure. *See* Kajihara, page 1500, section III. A., next to last paragraph. In contrast, in the present invention, redundant test stimuli is eliminated *after* selection of essential test stimuli.

Moreover, Applicants respectfully submit that Kajihara targets essential faults and does not select essential test stimuli.

Further still, in Kajihara, a pattern that is different from the original test pattern set is generated. In contrast, the present invention does not correct, change, or add a pattern, although a pattern in the original test pattern set can be deleted.

Therefore, the above-identified claims of the present invention are patentable over the reference, as the reference fails to teach each and every element of the claims. As dependent claims 2-5 and 7-9 depend from independent claim 1, the dependent claims are patentable over the reference for at least the reasons presented for the independent claims.

As dependent claim 6 depends from independent claim 1, Applicants respectfully submit that claim 6, via claim 1, is patentable over Kajihara, as Kajihara teaches away from the present invention. In particular, in contrast to the present invention, in Kajihara, the procedure relating to redundant tests occurs before the essential faults procedure.

Applicants respectfully submit that new claim 14 is patentable over the reference, as the reference does not teach or suggest, "selecting essential test stimuli; and eliminating redundant test stimuli after selection of said essential test stimuli," as recited in claim 14.

Applicants respectfully submit that the claims of the present invention are not taught, disclosed or suggested by the reference. The claims are therefore in a condition suitable for allowance. An early Notice of Allowance is requested.

If any further fees, other than and except for the issue fee, are necessary with respect to this paper, the U.S.P.T.O. is requested to obtain the same from deposit account number 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 4-11-06

By: _____
Reginald D. Lucas
Registration No. 46,883

1201 New York Avenue, NW, Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501